CLAIMS

What is claimed is:

1. Apparatus for wireless synchronization of electronic article surveillance systems, reducing the need for manual adjustment of transmitter timing by continually adapting and updating timing automatically to changing environmental conditions, comprising:

a first phase locked loop including:

means, responsive to a power line zero crossing, for detecting a line phase error;

a first numerically controlled oscillator responsive to said line phase error and to a crystal oscillator, said first numerically controlled oscillator and having a reference output, said reference output being an input to said line phase error means; and,

a second phase locked loop including:

means, responsive to a transmit signal from a first electronic article surveillance system, for detecting a transmit phase error; and,

a second numerically controlled oscillator responsive to said transmit phase error and said reference output; said second numerically controlled oscillator having a synchronized transmit output, said synchronized transmit output being an input to said transmit phase error means; and,

wherein said synchronized transmit output being usable as a trigger for synchronized transmission of a second electronic article surveillance system.

2. The apparatus of claim 1 further comprising means for filtering said line phase error wherein said first numerically controlled oscillator being responsive to a filtered line phase error and means for filtering said transmit phase error wherein said second numerically controlled oscillator being responsive to a filtered transmit phase error.

3. The apparatus of claim 2 wherein said first phase locked loop further comprises:

a counter responsive to said crystal oscillator;

a readable capture register responsive to said power line zero crossing and to an output of said counter, said readable capture register output being said line phase error;

a processor responsive to said power line zero crossing, to said line phase error, and to a power line phase locked loop interrupt, said processor selecting a value for a programmable period register;

comparator means for comparing the output of said counter and the value of said programmable period register, said comparator means further including means for resetting said counter and for sending said power line phase locked loop interrupt to said processor.

4. The apparatus of claim 3 wherein said second phase locked loop further comprises a counter having an output and comparator means for comparing said counter output to each of four programmable registers and generating four compare interrupts.

5. A method for wireless synchronization of electronic article surveillance systems, reducing the need for manual adjustment of transmitter timing by continually adapting and updating timing automatically to changing environmental conditions, comprising:

detecting a power line zero crossing and a reference output from a first numerically controlled oscillator to provide a line phase error signal;

said first numerically controlled oscillator receiving said line phase error signal and an oscillator signal and generating said reference output; and,

detecting a transmit signal from a first electronic article surveillance system and a synchronized transmit output from a second numerically controlled oscillator to provide a transmit phase error;

said second numerically controlled oscillator receiving said transmit phase error and said reference output and generating said synchronized transmit output, wherein said synchronized transmit output being usable as a trigger for synchronized transmission of a second electronic article surveillance system.

6. The method of claim 5 further comprising filtering said line phase error and filtering said transmit phase error.

7. A transmitter phase locked loop controller adapted for wireless synchronization of electronic article surveillance systems, reducing the need for manual adjustment of transmitter timing by continually adapting and updating timing automatically to changing environmental conditions, comprising:

means for ranking the energy received from an electronic article surveillance system in each of a plurality of adjacent timing windows;

means for selecting a coarse control algorithm if an energy rank of the first window is much greater than the fourth window but a rank index is not equal to 0 or 1;

means for selecting a medium control algorithm if the energy rank of the first window is much greater than the fourth window and the rank index is equal to 0 or 1, but the second and the third window are not substantially equal; and,

means for selecting a fine control algorithm if the energy rank of the first window is much greater than the fourth window and the rank index is equal to 0 or 1 and the second and the third window are substantially equal, said fine control algorithm running a lock detection algorithm.

8. The apparatus of claim 7 further including integrator means for incrementing or decrementing an integrator corresponding to no signal and too many signals, respectively.

9. The apparatus of claim 7 wherein said lock detection algorithm comprises:

means for setting a first flag if an early window is approximately equal to a late window;

means for setting a second flag if a highest energy window is relatively early or late;

means for setting a third flag if a second highest energy window is relatively early or late;

means for setting a fourth flag if most of the energy received is contained within relatively early or relatively late windows;

means for combining said flags to an index value equal to 8 times said first flag plus 4 times said third flag plus 2 times said second flag plus said fourth flag;

a lookup table providing a lock integrator update value associated with said index value;

means for updating a lock integrator with said lock integrator update value, including limiting said lock integrator to between 0 and a preselected maximum;

means for setting a lock threshold value to a low or a high value corresponding to whether a phase locked loop lock status is in a locked or an unlocked state, respectively; and,

means for setting said lock status to the locked state if said lock integrator exceeds said lock threshold value, and setting the lock status to the unlocked state and resetting said lock integrator if said lock integrator does not exceed said lock threshold value.

10. An antenna combiner for combining a plurality of antenna outputs for a transmitter phase locked loop adapted for wireless synchronization of electronic article surveillance systems, comprising:

means for setting a combiner lock status to an unlocked state if none of a plurality of antennas each having an antenna lock status are in a locked state;

means for ranking all antennas sampled in a current time slot according to the ratio of the largest energy window to the third largest energy window (SNR1) if the combiner lock status is in the locked state;

means for ranking only antennas in a locked state and sampled in said current time slot according to SNR1;

means for identifying one of said plurality of antennas having the highest SNR1 and a ratio of the largest energy window to the fourth largest energy window (SNR2) of at least 20dB;

means for adjusting a phase of the transmitter phase locked loop in relation to the output of the antenna identified by said identifying means and not adjusting the phase of the transmitter phase locked loop if no antenna is identified by said identifying means; and,

means for setting said combiner lock status to the antenna lock status of the antenna is identified by said identifying means.

11. A method for adapting a transmitter phase locked loop controller for wireless synchronization of electronic article surveillance systems, reducing the need for manual adjustment of transmitter timing by continually adapting and updating timing automatically to changing environmental conditions, comprising:

ranking the energy received from an electronic article surveillance system in each of a plurality of adjacent timing windows;

selecting a coarse control algorithm if an energy rank of the first window is much greater than the fourth window but a rank index is not equal to 0 or 1;

selecting a medium control algorithm if the energy rank of the first window is much greater than the fourth window and the rank index is equal to 0 or 1, but the second and the third window are not substantially equal; and,

selecting a fine control algorithm if the energy rank of the first window is much greater than the fourth window and the rank index is equal to 0 or 1 and the second and the third window are substantially equal, said fine control algorithm running a lock detection algorithm.

12. The method of claim 11 further including incrementing or decrementing an integrator corresponding to no signal and too many signals, respectively.

13. The method of claim 11 wherein running said lock detection algorithm comprises:

setting a first flag if an early window is approximately equal to a late window;

setting a second flag if a highest energy window is relatively early or late;

setting a third flag if a second highest energy window is relatively early or late;

setting a fourth flag if most of the energy received is contained within relatively early or relatively late windows;

combining said flags to an index value equal to 8 times said first flag plus 4 times said third flag plus 2 times said second flag plus said fourth flag;

looking up in a table a lock integrator update value associated with said index value;

updating a lock integrator with said lock integrator update value, including limiting said lock integrator to between 0 and a preselected maximum;

setting a lock threshold value to a low or a high value corresponding to whether a phase locked loop lock status is in a locked or an unlocked state, respectively; and,

setting said lock status to the locked state if said lock integrator exceeds said lock threshold value, and setting the lock status to the unlocked state and resetting said lock integrator if said lock integrator does not exceed said lock threshold value.

14. A method for combining a plurality of antenna outputs for a transmitter phase locked loop adapted for wireless synchronization of electronic article surveillance systems, comprising:

setting a combiner lock status to an unlocked state if none of a plurality of antennas each having an antenna lock status are in a locked state;

ranking all antennas sampled in a current time slot according to the ratio of the largest energy window to the third largest energy window (SNR1) if the combiner lock status is in the locked state;

ranking only antennas in a locked state and sampled in said current time slot according to SNR1;

identifying one of said plurality of antennas having the highest SNR1 and a ratio of the largest energy window to the fourth largest energy window (SNR2) of at least 20dB;

adjusting a phase of the transmitter phase locked loop in relation to the output of the antenna identified by said identifying means and not adjusting the phase of the transmitter phase locked loop if no antenna is identified by said identifying means; and,

setting said combiner lock status to the antenna lock status of the antenna is identified by said identifying means.

15. An electronic article surveillance system incorporating wireless synchronization of a plurality of electronic article surveillance systems, reducing the need for manual adjustment of transmitter timing by continually adapting and updating timing automatically to changing environmental conditions, comprising:

an electronic article surveillance transmitter and receiver and at least one antenna connected to the transmitter and receiver, said transmitter including:

a first phase locked loop including:

means, responsive to a power line zero crossing, for detecting a line phase error;

a first numerically controlled oscillator responsive to said line phase error and to a crystal oscillator, said first numerically controlled oscillator and having a reference output, said reference output being an input to said line phase error means; and,

a second phase locked loop including:

means, responsive to a transmit signal from a first of a plurality of electronic article surveillance systems, for detecting a transmit phase error; and,

a second numerically controlled oscillator responsive to said transmit phase error; said second numerically controlled oscillator having a

synchronized transmit output, said synchronized transmit output being an input to said transmit phase error means; and,

wherein said synchronized transmit output being usable as a trigger for synchronized transmission of a second of said plurality of electronic article surveillance systems.